उच्च तीव्रता प्रोटॉन त्वरक

9

संदर्भ चरण उत्पादन प्रणालियाँ

*सुजो सी. आई., सत्यम रावत और गोपाल जोशी
त्वरक नियंत्रण प्रभाग, भाभा परमाणु अनुसंधान केंद्र (भापअ केंद्र), ट्रांबे-400085, भारत

325 MHz रेफरेंस फेज जनरेशन सिस्टम

सारांश

त्वरक नियंत्रण प्रभाग, भाभा परमाणु अनुसंधान केंद्र, ने भारतीय संस्थानों और फर्मीलाब के बीच विज्ञान और प्रौद्योगिकी सहयोग (आईआईएफसी) के तहत लो-लेवल रेडियो आवृत्ति नियंत्रण प्रणालियाँ विकसित की हैं, जिनमें एक अप-कन्वर्टर, एक डाउन-कन्वर्टर, एक रेफरेंस फेज जनरेशन प्रणाली, और एक डिजिटल सिग्नल प्रोसेसिंग (डीएसपी) मॉड्यूल शामिल हैं। रेफरेंस फेज जनरेशन प्रणाली एक स्थिर रेडियो आवृत्ति रेफरेंस उत्पन्न करता है, जो त्वरक कैविटी में रेडियो आवृत्ति तरंगों के फेज-नियंत्रण के लिए आवश्यक होता है, साथ ही एक लोकल-ऑस्सीलेटर (एलओ) सिग्नल प्रदान करता है जो आवृत्ति के रूपांतरण के लिए उपयोग होता है, और डीएसपी मॉड्यूल में उपयोग किए गए एफपीजीए के लिए एक क्लॉक सिग्नल भी प्रदान करता है। कैविटी के भीतर रेडियो आवृत्ति तरंगों के एंप्लिटूड और फेज की स्थिरता सुनिश्चित करने के लिए, रेफरेंस फेज सिग्नल, एलओ, और क्लॉक सिग्नल में अत्यंत कम फेज नॉइज़ बनाए रखना आवश्यक है। इसके लिए प्रणाली का तापीय स्थिरीकरण आवश्यक है ताकि अवयवों में तापमान परिवर्तनों के कारण फेज ड्रिफ्ट को कम किया जा सके। इस लेख में आईआईएफसी के तहत विकसित 325 मेगाहट्र्ज और 650 मेगाहट्र्ज रेफरेंस फेज जनरेशन प्रणाली की डिज़ाइन, कार्य सिद्धांत, परीक्षण परिणाम, और वर्तमान स्थिति का संक्षिप्त अवलोकन प्रस्तुत किया गया है।

High Intensity Proton Accelerator

9

Reference Phase Generation Systems

***Sujo C. I., Satyam Rawat and Gopal Joshi**
Accelerator Control Division, Bhabha Atomic Research Centre (BARC), Trombay-400085, INDIA

325 MHz Reference phase generation system.

ABSTRACT

Accelerator Control Division, Bhabha Atomic Research Centre has developed Low-Level RF control systems, each comprising of an up-converter, a down-converter, a reference phase generation system, and a digital signal processing (DSP) module under the Indian Institutions and Fermilab Collaboration (IIFC). The reference phase generation system generates a stable RF reference for phase-control of RF fields in an accelerator cavity, a local-oscillator (LO) signal for frequency translation, and a clock signal for FPGA on-board the DSP module. To ensure the stability of both the amplitude and phase of RF fields within the cavity, it is essential to maintain an ultra-low phase noise in the reference phase signal, LO, and clock signals. This requires thermal stabilization of the system to reduce phase drifts caused by temperature changes in the components. This article gives a brief overview of design, working principles, test results, and present status of the 325 MHz and the 650 MHz reference phase generation system developed under IIFC.

KEYWORDS: *Reference phase generation, Phase noise, Phase averaging.*

**Author for Correspondence: Sujo C. I.*
E-mail: sujo@barc.gov.in

Introduction

Proton Improvement Plan (PIP-II), Fermilab, USA is a high intensity proton accelerator which includes five different types of superconducting cavities with resonant frequencies at 162.5 MHz, 325 MHz, and 650 MHz. ACnD, BARC has developed LLRF systems for 325 MHz and 650 MHz cavities with technical support and guidance from Fermilab under IIFC. A 650 MHz LLRF control system has been commissioned at the Horizontal test facility (HTS), RRCAT. Additionally, two LLRF systems have been delivered to Fermilab to be tested with 325 MHz and 650 MHz RF cavities. A 325 MHz reference phase generation system has been developed as part of LLRF system. This system generates a phase-synchronized 325 MHz RF reference signal, a 345 MHz LO signal for up/down converters, and a 1320 MHz clock signal for the FPGA on-board the DSP module. Similarly, a 650 MHz reference phase system has also been developed, producing a 650 MHz reference signal, a 670 MHz LO signal, and a 1320 MHz FPGA clock signal.

Design of Reference Phase Generation Systems

The 325 MHz reference phase generation system utilizes a 325 MHz crystal oscillator as its RF source, which has an excellent phase noise characteristic. The phase noise of the crystal oscillator is -164.7 dBc/Hz at an offset of 10 kHz. Additional RF signals at various frequencies are derived from this crystal oscillator. To achieve this, RF frequency multipliers, frequency dividers, low-noise amplifiers, and single-sideband mixers with minimal additive phase noise have been carefully selected and integrated to generate the derived RF signals. The 650 MHz reference phase module utilizes the reference output from the 325 MHz reference phase system as its RF source. The reference phase generation systems also produce a 1300 MHz RF signal for utilization by beam instrumentation systems. When selecting RF amplifiers, it is essential to consider the length of the reference phase signal distribution line and the cable loss incurred over its entire length. The 325 MHz and 650 MHz reference phase generation systems are depicted in Fig.1 and 2, respectively.

Table 1 and 2 present the phase noise measurement results for various signals in the 325 MHz and the 650 MHz reference phase generation systems, respectively.

Fig.3 displays the phase noise spectral density of 1320 MHz FPGA clock signal derived from the 325 MHz master oscillator signal using frequency multipliers and single-sideband mixers. The single-sideband mixer utilizes RG 405 phase-matched coaxial cables to mitigate the quadrature phase errors resulting from temperature variations.

Fig.1: 325 MHz reference phase generation system.

Fig.2: 650 MHz reference phase generation system.

Table 1: Test results of 325 MHz reference phase generation system.

RF signal	Signal Level	Phase noise at 100 kHz offset
325 MHz reference output signal	7.9 dBm	-166 dBc/Hz
345 MHz LO signal	16.0 dBm	-148 dBc/Hz
325 MHz reference output signal to 650 MHz system	13.1 dBm	-163 dBc/Hz
1320 MHz clock signal	12.2 dBm	-149 dBc/Hz

Table 2: Test results of 650 MHz reference phase generation system.

RF signal	Signal Level	Phase noise at 100 kHz offset
650 MHz reference output	10.2 dBm	-157 dBc/Hz
670 MHz LO signal	16.7 dBm	-142 dBc/Hz
1300 MHz reference signal	7.9 dBm	-151 dBc/Hz
1320 MHz clock signal	16.8 dBm	-152 dBc/Hz

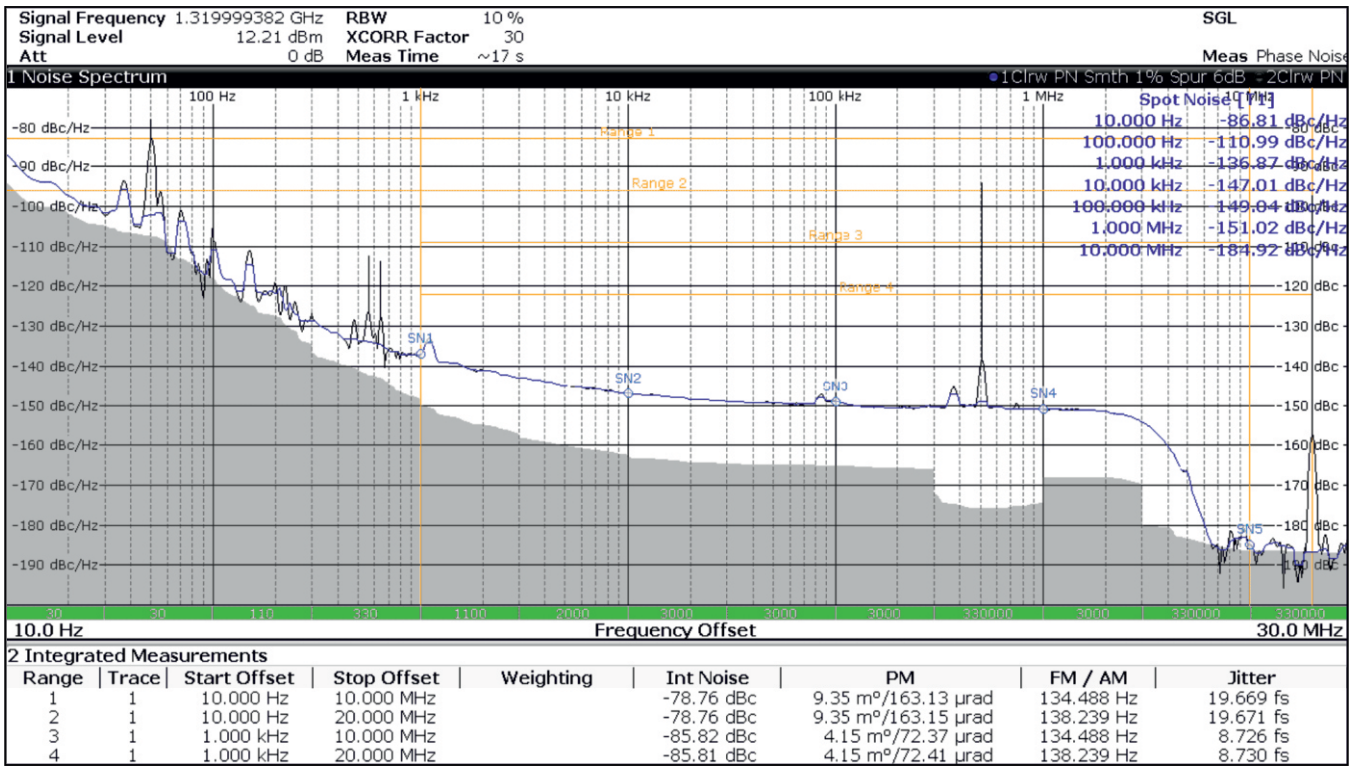

Fig.3: Phase noise spectral density of 1320 MHz FPGA clock signal.

Phase Averaging: Mitigating Phase Drifts Caused by Temperature Variation

At Fermilab, the length of the phase reference signal distribution cable, within each frequency section, spans nearly 100 meters. Variations in ambient temperature cause changes in the length of the distribution cable, thereby altering the phase of the RF reference signal. To mitigate this phase change resulting from temperature variation, the phase averaging method [1] is employed. In this method, a standing wave is induced in the reference line by introducing a short at the end of the transmission line. At any point along the reference line, both forward and reflected waves are extracted using a bi-directional coupler. The amplitudes and phases of these waves are carefully adjusted to maintain near-identical values. These adjustments are achieved through the use of variable attenuators and phase shifters. Subsequently, the two waves are combined. As long as the phase of the shorted end remains constant, the phase of the combined signal remains unaffected by changes in length, and thus, temperature. To ensure stability at the shorted end of the cable, a phase-locked loop is employed. This entire mechanism helps to maintain the phase stability of the reference signal which is an essential requirement in a LLRF system.

Temperature Stabilisation of the Reference Phase Generation System

To mitigate phase drift in the components resulting from ambient temperature variations (expected to range from 19°C to 35°C at Fermilab), the temperature of the reference phase generation system is regulated at 40°C. This is achieved through the development of heater PCBs, featuring long traces of copper uniformly distributed on an FR-4 substrate. All RF components are mounted on an aluminum plate, with the heater PCBs positioned beneath it. Thermally conductive acrylic interface pads, known as heat pads, are placed between the heater PCBs and the aluminum plate to enhance heat transmission. Temperature measurement is facilitated by a resistance temperature detector (RTD), Pt100, which is interfaced with a temperature controller. A 32V, 30A DC power supply is used to provide current to the heater PCBs. Fig.4 illustrates the heater PCBs with heat pads. It requires nearly 100 W of DC power to maintain the temperature of the reference phase generation system at 40°C (with a room temperature of 27°C).

Fig.4: Heater PCBs with heat pads.

Present Status

Based on the experimental results showing compliance with the given system specifications, the shipment of the reference phase generation systems to Fermilab was approved. Both 325 MHz and 650 MHz systems have already been sent to Fermilab for testing with 650 MHz and 325 MHz cavities. Commissioning of these systems is awaited.

Acknowledgement

The authors sincerely acknowledge and appreciate the technical support received from Fermilab during the design, fabrication, and testing phases. Additionally, the authors would like to thank all colleagues at ACnD for their invaluable support throughout the project.

References

[1] B. Chase, E. Cullerton, "1.3 GHz Phase Averaging Reference Line for Fermilab's NML ASTA Program", Beams-doc-3806-v2.

[2] M. Afaash, et al., "Reference Phase Distribution Scheme and Test Results for SSR1 under IIFC," Proceedings of the 2019 International Particle Accelerator Conference (InPAC), IUAC, New Delhi, 2019.