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# COMPACT 8 K MULTI-CHANNEL ANALYZER WITH USB INTERFACE AND MULTI-MODE OPERATION

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**Abstract**

*A Multi-Channel Analyzer (MCA) is the heart of a nuclear spectroscopy system. The paper describes a new, high-performance MCA with many advanced features. Some of them are in-built hardware for List and MCS modes in addition to the standard PHA mode of operation, local spectrum memory and USB bus interface. The mode of operation is selectable through GUI. The MCA uses an FPGA to integrate all the digital circuits in one chip and it has state-of-the-art analog chips in analog side for superior performance. The resolution is selectable from 256 channels to 8 K channels suitable for all needs. It supports good input pulse rate (typically more than 100 KHz) without significant dead time penalty. The USB bus interface offers a truly universal and simple connectivity with almost any modern PC or Simputer for MCA data manipulation, control and display. The applications of the MCA include energy spectroscopy, half-life analysis and analysis of individual events and it is a good fit for embedded and battery-operated instruments as well as for standard desktop instruments.*

## Introduction

An MCA is a major part of nuclear spectroscopy systems. Depending on the application, it is used in either PHA or MCS or List mode of operation. The MCA presented here, supports all of them in one system and it is satisfactorily working as per the specifications in the real world. The digital circuitry which includes control registers, timers, sequencer, memory controller, 8 bit generic bus interface and ADC linearization circuits, etc. is designed using VHDL with 200 K gates FPGA. The analog part of the circuit uses state-of-the-art analog chips like low power, high speed and high precision comparators, op-amps, ADC and DAC. It utilizes the isolated power supplies using DC-DC converters and regulators, which run only on +5V input supply. Use of isolated power supplies and ground also scales down the effect of noise associated with feeding power supply,

resulting into superior performance. The PHA (Pulse Height Analysis) mode is the most common mode of operation. Here the incident pulses are counted in individual memory channels depending on their energy and the plot of *count vs. energy* is available after the experiment. This PHA mode is useful for isotope identification, calibration and nuclear spectroscopy experiments. The MCA supports 256 to 8 K channels resolution with a DNL of better than + 1 % at 8 K, and has a fixed conversion time of 7 ms.

The MCS (Multi-Channel Scaling) mode records the counting rate of events as a function of time. The count is recorded for each *dwell time* slice and is stored in memory at incremental channel locations. It is useful for isotope half-life analysis. The MCA supports 32K channels length of MCS with dwell time of 4 ms to 4000 s. It has an internal dwell timer as well as provision of external channel incrementing pulse. In the List mode, the energy (amplitude) information of individual event is recorded at incremental memory locations. It is useful for analysis of individual events with respective to time or any other variable. The MCA supports a list of 32 bit into 32 K optional support for individual data tagging to create 2D spectrums.

## Design methodology

The following are the few aspects of the MCA design presented here:

- Low power precision analog design
- Low power, fully synchronous digital design
- Generic and portable VHDL code, independent of FPGA platform
- Hierarchical
- Power-down mode for SRAM memory

## Functional Brief

The block schematic of MCA card is shown in Fig.1. The analog circuit consists of LLD and ULD comparators, peak stretcher and peak detect comparator, 16-bit successive approximation ADC and DAC for sliding scale correction. When the input pulse height exceeds the lower level discriminator (LLD) threshold, the peak stretcher is enabled. It stores the peak amplitude of

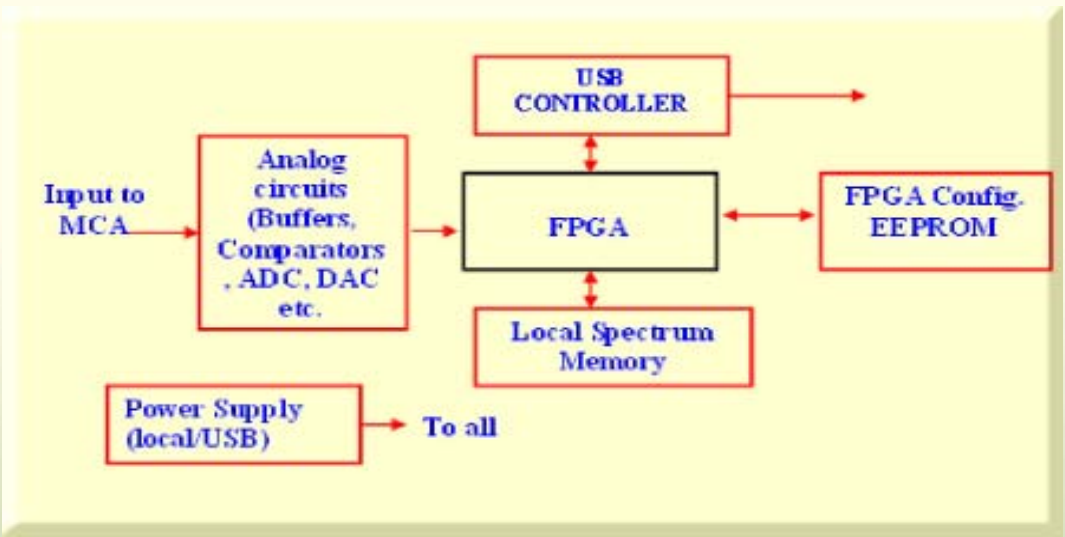



**Fig. 1 : Block diagram of the MCA**

the input pulse. If the input pulse amplitude falls within the LLD and ULD thresholds, the control and logic circuit is enabled and the ADC conversion process starts. The required mode of the MCA operation (*PHA*, *MCS*, or *List*) is selected through the GUI and accordingly the internal sequencers and other digital circuitry processes the ADC data.

## PHA operation

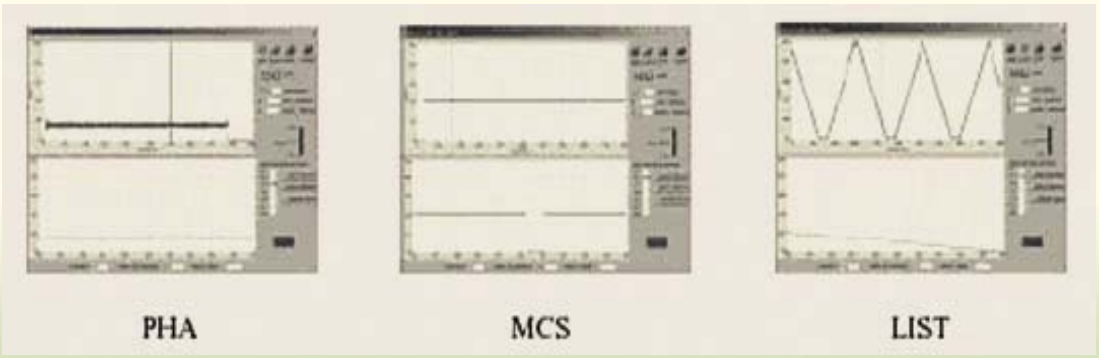
The ADC code corresponding to the specific input pulse amplitude is used as a memory address pointer and the 31-bit count value stored at the memory location is incremented by 1. This is done on "byte by byte" basis to speed-up the process of spectrum building and to maintain 8-bit bus interface. The process typically takes a minimum of 400 ns to a maximum of 1.6 μs, depending on the number of byte access (1,2, 3 or 4). This process is parallel with the ADC conversion time (5 μs max), using a 1 stage buffer and thus the dead time is minimized.

incremented. The counter then starts fresh counting for next channel. The process continues for the 32 K channels or the acquisition time set. The process can be interrupted by external TTL input of MCS reset, which resets the channel pointer to 0 and restarts from channel 0.

## List operation

The ADC data is written in the first channel in the memory and the channel pointer is incremented to next. The next data from the ADC is written there. This process repeats for 32 K channel length, which can store the energy information for 32 K events.

The screen-shots below show the data acquired in various modes with input from a sliding pulse generator:




## MCS operation

An internal 32-bit counter counts the input pulses validated by LLD and ULD (SCA) for the duration of the *dwell time*, and then the count is written in the first channel in the memory and the channel pointer is

## Bus arbitration logic

The MCA has a memory management with bus arbitration logic for single port SRAM chip. It resolves the Read / Write requests from ADC side and PC side, giving higher priority to the ADC side, so that the histogram doesn't

miss any input event. The PC side read request is processed intermittently and is notified by raising a flag bit embedded as a MSB bit of the 32-bit channel count. The maximum resolution supported by the digital hardware is 32 K channels of 31 bits each for future expansion, but presently, the maximum resolution available is 8 K channels. The on-board histogram memory makes the hardware to operate independently, once initialized and thus doesn't require frequent PC access. The SRAM reset function is user driven through GUI, so that the spectrum is protected from automatic erasing.

## USB bus interface

The MCA has an on-board USB controller chip. It supports a data transfer rate of 12 MBPS and provides an excellent connectivity with most of the new PCs and palm-top type computers like *Simputer*, which helps make a compact and portable spectroscopy system.

## Specifications

Following are the specifications for the MCA:

1. PHA mode:
   - MCA resolution : 256, 512, 1K, 2K, 4K and 8K channels
   - Spectrum memory : 128 K Bytes single port SRAM
   - Max counts / channel : 31 bit (2 Giga counts)
   - Pulse processing time : 7 $\mu$s
   - Pile up rejection : Active high TTL input
   - DNL : + 1 % at 8K resolution
   - INL : + 0.05 % F.S.
2. LIST mode:
   - List size : 32 K x 32 bit
   - Pulse processing time : 7 $\mu$s
   - Supports all PHA controls : Yes
3. MCS mode:
   - Input (through SCA) : 100 KHz max, single channel
   - Memory length (channels) : 32 K
   - Max counts / channel : 31 bits (2Giga counts)
   - Channel increment : External TTL pulse or internal dwell timer
   - Dwell timer setting : 4 $\mu$s to 4000 seconds, set through software
4. Common specifications:
   - MCA Input : Single channel, 0 to +10 volts
   - Timer : 32 bit, integrated in FPGA
   - Preset Time : LIVE or CLOCK, $2^{32}$ seconds (136 yrs) max.
   - ADC conversion time : 5 $\mu$s
   - LLD, ULD, Baseline : Set through on-board DACs using application GUI
   - Power requirement : 5V, ~ 500 mA

## Future Plans

The digital part of the MCA may be transformed into indigenous digital ASIC to replace the FPGA and to make the system lower power and more compact as well as self-reliant. The analog circuits may be replaced with indigenous analog hybrid circuits to make it more compact.

## References

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2. Radiation Detection and Measurement by G. F. Knoll.
3. Xilinx Data Book CDROM 2003.
4. Technical Manual of MCA-2000, Electronics Division, BARC.

# ABOUT THE AUTHORS

**Mr C.P. Kulkarni** did his BE (Electronics) from Shivaji University in 1995. He joined 39th batch of training school. After training, he was posted in Electronics division in 1996. He has developed a variety of MCAs and spectroscopy systems for different applications. His major areas of work include FPGA based system design and development of nuclear instruments for embedded and portable systems. Currently, he is working on the development of ASICs for MCAs.

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Mr M.D. Ghodgaonkar obtained his M. Sc. (Physics) from the University of Indore and joined Electronics Division in 1969 after the completion of 12th batch of BARC Training School. His contributions to Nuclear Instrumentation program over the last 37 years include Neutronic instrumentation (Purnima, FBTR and Cirus and Apsara upgradation), Transputer based Parallel Processing for nuclear applications, CAMAC Instrumentation for Accelerator control systems (FOTIA and LINAC) and high performance Multi-parameter systems for Nuclear Research. He has been instrumental in establishing the indigenous development of CAMAC instrumentation. During IX plan, he initiated the development of ASICs and Hybrids, which is being rigorously pursued. He has several publications in the filed of nuclear instrumentation. At present he heads Electronics Division of BARC and his current electronics interests are indigenous development of ASICs, radiation detectors, embedded instrumentation for radiation monitors and front end electronics for physics experiments, High speed high throughput Data Acquisition Systems and Radiation Security Instrumentation relevant to DAE programs.

Dr S. K. Kataria obtained his B.Sc. Degree from Rajsthan University in 1965 (Gold Medalist in Physics) and completed the BARC Training School Course in 1966 as Homi Bhabha Awardee. He did his postgraduate degree and doctoral work in the area of experimental nuclear physics. For three decades, he worked in the area of nuclear experimental studies and nuclear instrumentation for accelerators and nuclear reactors while in NPD, BARC. Since the last decade, he has been working with a mission of modernisation of Electronics and Radiation Detectors and related Instrumentation. During this period he has led the development of new radiation detectors, HMCs, and ASICs for nuclear electronics, bio-medical and reactor instrumentation. He has published over 120 research papers in journals of international repute and over 200 in national and international symposia. He retired as an Associate Director, E&I Group of BARC and is at present Raja Ramanna Fellow at the Electrical Engineering Department, IIT Mumbai with the aim to promote collaborative development programs in these areas amongst DAE Institutes and IIT Bombay.