Chapter 10

Design of Electrostatic Parameters and Vacuum Transmission Line for LTD-1 MV Module

––*Sukanta Kumar Mishra, Partha Banerjee*

Linear Transformer Driver development started at High Current Electronics Institute (HCEI), Russia. Later it was adopted by leading research institutes of USA and China. An LTD module consists of an array of cavities in series and each cavity consists of multiple units called bricks connected in a circular fashion and all are in parallel. High current is achieved from parallel bricks of single cavity and high voltage is generated by connecting multiple cavities in series. A single brick consists of energy storage capacitor, spark gap switch and magnetic core that is common to all the bricks in the cavity. The capacitors transfer the energy to the secondary matched load via the switch and transformer action [1]. The main advantage of LTD topology is that the compressed pulse (nanosecond duration) is produced in the same stage (as the brick element decides the output pulse width). Where as in Marx generator which also produce high voltage and current pulsed power, multiple stages of bulky, voluminous oil/water tanks pulse forming line is required to compress the microsecond pulse output of the Marx generator to nanosecond duration pulse [2].

10.1. Introduction

The proposed 3 MV LTD module is divided into 30 stage/ cavity & each cavity should be able to generate 100 kV across matched 1 Ω load. The module is proposed to develop in 3 phases as: LTD-1, LTD-2 and LTD-1 MV system. LTD-1 and LTD-2 have been developed to understand LTD concept, synchronous triggering of multiple switches and voltage addition with multiple cavities. Development of LTD-1 and LTD-2 has been discussed in separate chapter. In LTD-2 and the proposed LTD-1 MV, the cavity part (electrostatic part) is having pressurized nitrogen as insulation and the voltage adder part is in vacuum. This makes our system unique as most of the developed LTD systems are having cavity parts oil insulated. LTD-1 and LTD-2 are overdesigned as they are made for learning purposes. To reduce the cavity size and to incorporate magnetic insulation transmission line (MITL) concept, LTD is redesigned for 1 MV output. It consists of 2 modules of each 500 kV, 100 kA, 60 ns output. Complete 500 kV module will be kept inside a single pressure chamber of 5 bar nitrogen pressure of total module length of 1000 mm. Later on such 500 kV modules will be cascaded to generate the required voltage (2 module for LTD-1 MV system and 6 modules for proposed 3 MV, 100 kA, 60 ns LTD module for radiographic application).

10.2. Electrostatic Component Selection for LTD-1 MV System

As mentioned earlier, it is proposed to develop a LTD module having output of 500 kV, 100 kA and 60 ns pulse width across critically matched load (5 Ω). Based on the insulation requirement and safe high voltage handling, the module is divided in to 5 stages/cavities which are connected in series. The output of each cavity will be 100 kV, 100 kA, and 60 ns pulse width across critically matched load impedance of 1 Ω. Based on the current rating of the capacitors, each cavity consists of 10 bricks in parallel to generate the required current of 100

kA. Each brick consist: two energy storage capacitors which are charged equal voltage of opposite polarity, an electrical triggered switch which can withstand 200 kV DC voltage and torroidal magnetic cores that are common to all bricks. Other important components of a cavity are charging resistors of each bricks that solve two purposes: acts as limiting resistor during charging and isolating each bricks for cross flow of energy during discharging. Trigger arrangement and trigger resistors for triggering of all switches with in a cavity.

10.2.1. Capacitor Selection

Capacitance value of the capacitor used in LTD-1 MV module can be calculated as given below. For each cavity, the required output is 100 kV, 100 kA, 60 ns pulse width across critically matched load (R) of 1 Ω. For critically matched load, $R = 2\sqrt{\frac{L_{total}}{C_{total}}} = 1\ \Omega$ and pulse width of 60 ns, ($0.8\pi\sqrt{L_{total}C_{total}} = 60$ ns). Where $C_{total} = \frac{xC}{2}$ and $L_{total} = \frac{L}{x}$; C is the capacitance of each capacitor of the brick. Since, two capacitors are connected in series in a brick, the equivalent capacitance of a brick is $\frac{C}{2}$. L is the total inductance of each brick which consist of capacitor equivalent series inductance (ESL), Sparkgap inductance and cavity inductance. x is the bricks number connected in parallel inside the cavity. For x=10, it is found that C_{total} = 48 nF, L_{total} = 12 nH. To accommodate loss factor inside the cavity, the total capacitance value is chosen as 60 nF. So each capacitor of the brick having capacitance value, $C = \frac{2C_{total}}{n}$ = 12 nF. To generate 100 kV peak output voltages from each cavity at critically matched load condition, DC charging voltage will be $\frac{100\ kV}{0.735} \approx 135$ kV. Considering losses, each capacitor pair i.e. brick of each cavity has to handle 160 kV to 180 kV. So each 12 nF capacitor of each brick will be DC charged to 80 kV to 90 kV. To generate 100 kA from each cavity and there are ten bricks are in parallel, so each capacitor of the brick will supply 10 kA at matched load conditions. So capacitor rating will be 12 nF, 100 kV, 10 kA.

10.2.2. Magnetic Core Selection

One of the major hardware components of the LTD cavity is the torroidal magnetic core that is common to all bricks in a cavity and it is placed in symmetric fashion in both polarity sides of the cavity. In pulsed power system where frequency is high, selection of core material is one of the most critical issues. Saturation flux density (B_s), Electrical resistivity is the important magnetic and electrical properties of the magnetic materials taken into consideration when selecting magnetic core [3]. In single pulse application, eddy current loss in the core is dominant. Eddy current loss can be treated as resistive loss in the core and can be electrically represented as resistor in parallel to the main load. The core should have high core resistance so that eddy current loss will be less and most of the stored energy in primary will be transferred to the secondary load. To have high core resistance, the core should have high electrical resistivity and low core tap thickness. The core should also have high saturable flux density (B_s) so that core size will be small since the size of the core is inversely proportional to saturable flux density

for a constant volt-second product. Based on the aforementioned parameters, Fe-amorphous alloy based core (equivalent to 2605SA1 of Metglas®) has been chosen as core material in our experiments. The material has B_s value of 1.56 T, electrical resistivity of 137 μΩ-cm and ribbon thickness of ~25 micron.

For an output voltage pulse of 100 kV and 60 ns pulse width of the single cavity, the cores used in the cavity should not saturate during 60 ns so that maximum stored energy gets transferred to the load. The output voltage of single cavity is plotted when the cavity capacitance (total 60 nF) is charged to 200 kV (±100 kV) in simulation. The cavity inductance is set as 12 nH for 60 ns pulse width (FWHM) and the stored energy of the cavity is transferred to critically matched load of 1 Ω in simulation parameters. The integration of the voltage ($\int V(t)dt$) for the complete time period (60 ns pulse width) is found to be 12 mV-Sec. This calculated voltage-time product is higher than the experimental one as the output voltage is considered as 135 kV (for critically matched load) in simulation whereas the actually output of each cavity will be 100 kV. This higher V-t product compensates the losses in magnetic material and low saturable flux density (B_s) from the experimental value. So for this V-t product core should not be saturated. Core area can be calculated from the Eq. (10.1) as,

$$\int_0^T V(t)dt = N \times A_m \times \Delta B \tag{10.1}$$

Where,

T = Time to core saturation,

V (t) = Output voltage in Volts,

$\Delta B = B_s\text{-}(-B_r)$ or $B_s\text{-}(-B_s)$: change in magnetic flux density in Tesla,

N = Number of turns,

From (Figure 10.1) A_m = Magnetic material cross section area = $\left(\frac{OD-I}{2}\right) \times h \times PF$ for toroidal core in m^2,

PF = Packing factor for the core. Generally 0.8 to 0.85.

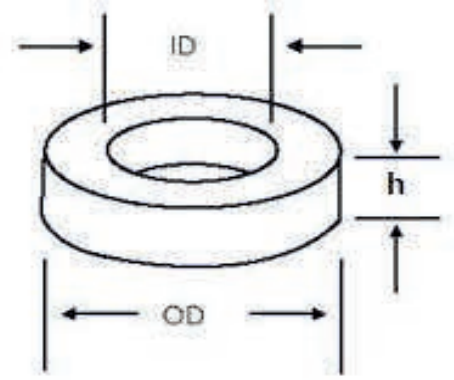


Figure 10.1. Schematic of torroidal Magnetic core.

For N = 1, $\int V(t)dt = 12$ mV-Sec, $\Delta B = 2$ Tesla, Total area of the magnetic core can be calculated in Eq. (10.2) as,

$$A_m = \frac{\int V(t)dt}{\Delta B} = \frac{12\times10^{-3}}{2} = 6\times10^{-3}\ \text{m}^2 = 60\ \text{cm}^2 \tag{10.2}$$

Two sets of core to be used in each polarity side for symmetry. Considering PF =0.8, core dimension can be calculated from Eqs. (10.3) and (10.4) as,

$$A_m = 2 \times \left(\frac{\text{OD}-\text{I}}{2}\right) \times \text{h} \times \text{PF} = 60\ \text{cm}^2 \tag{10.3}$$

$$(\text{OD-ID}) \times \text{h} = 75\ \text{cm}^2 \tag{10.4}$$

Core height can be selected based on the capacitor height so that it will be easy to keep insulator plate on top of capacitor and core azimuthally for insulation purpose from return path from ground. So for h = 45 mm, Outer Diameter (OD)-Inner Diameter (ID) = 168 mm.

Core outer diameter can be calculated considering Figure 10.2 and Eq. (10.2) as,

$$\text{Core OD} = \frac{\text{x}(\text{C}_\text{w}+\text{d})}{\pi} - 2\text{Y} \tag{10.5}$$

Where,

x = Number of bricks in a cavity

C_w =Capacitor width in mm

d = gap between two capacitor in mm

Y = gap between capacitor and core in mm

Considering C_w = 150 mm, d= 50 mm & Y = 50 mm,

Core OD = 537 mm

For (OD-ID) = 168 mm,

Core ID = 369 mm & core height = 45 mm

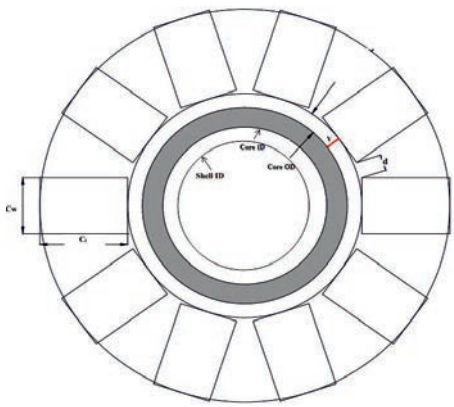


Figure 10.2. Schematic of single cavity

Considering a gap of 50 mm between core and bore ID of LTD, Bore ID/Vacuum flange ID is calculated to be 269 mm. The vacuum flange ID will be the input for the design of Magnetic Insulation Transmission Line (MITL) for the voltage adder part.

10.2.3. Spark Gap Switch Parameter Selection

The main challenge associated in successful realization of the LTD scheme is the simultaneous firing of large number of spark gap switches (10 numbers per cavity in our case) that are used to transfer the stored energy in the capacitors to a given load. The individual switches should have stable breakdown characteristics (voltage withstand capability of ≥ 200 kV, should have low pre-fire probability), low inductance and less electrode erosion. Three electrode field distortion switch (each having height of 100 mm and outer diameter of 100 mm with two main electrodes and one trigger electrode) is proposed to be used in the cavities of LTD-1 MV system. The switch dimensions are chosen to reduce the brick size. Selection of electrode profile is based on experimental study. The switch parameters can be summarized as (i) Charge voltage: 200 kV, (ii) Peak current: 50 kA, (iii) Insulation: pressurized dry nitrogen gas, (iv) Electrode material: SS or W-Cu alloy, (v) Trigger by 100 kV pulse having dV/dt rating > 5 kV/ns, (vi) Pre-fire rate ≤ 5% (vii) Lifetime ≥ 5000 shots (viii) Diameter ≤ 10 cm (ix) Length ≤ 10 cm.

10.3. Vacuum Transmission Line Design

The electrostatic design part is taken as input for the design of vacuum coaxial section of LTD-1MV. Individual cavity voltage (100 kV) and equivalent impedance (1 Ω) are taken as input for the design along with bore inner diameter (269 mm) and cavity gap (20 mm). Other constraints for the design of inner shell are: (i) Inner shell diameter is constant through-out the module, (ii) Inner shell diameter in a module is fixed at required diameter of the end cavity of the module and (iii) total 5 cavities per module.

10.3.1. Feasibility of Positive Adder Design

With these inputs and from electric field (E) coaxial impedance (Z) Eqs. (10.6) and (10.7), we get inner shell diameter as given in Table 10.1.

$$E = \frac{2V_0}{D_0 \times \ln(\frac{D_1}{D_0})} \tag{10.6}$$

$$Z = 60 \times \ln(\frac{D_1}{D_0}) \tag{10.7}$$

Where V_0 is the module voltage in kV, D_1 and D_0 are the bore inner diameter and inner shell diameter respectively. The inner shell diameter is chosen to match the vacuum impedance of end cavity of each 500 kV module. So, for bore diameter (D_1) 269 mm, the electric field goes beyond 20 kV/mm in the first module itself which is the maximum permitted vacuum electric field emission. Thus, we infer, the positive adder topology can't be adopted for LTD-1 MV.

Table 10.1. Inner shell diameter for positive adder.

End cavity No.	Vacuum impedance (Z) in Ω	Module voltage (V_0) in MV	Inner shell diameter (D_0) in mm	Module E-field (E) in kV/mm
5	05	0.5	247	48
10	10	1.0	228	53
15	15	1.5	209	57
20	20	2.0	193	62
25	25	2.5	177	63
30	30	3.0	163	73

10.3.2. Negative Adder & MITL Topology

In negative adder, the inner shell is negative cathode, the outer shell (bore inner diameter) is positive anode. Very large electric field, present in these devices, causes electron emission, ectons [4] from cathode and causes voltage breakdown and thereby forming plasma channel. But, in negative adder, electrons emitted from cathode can be streamlined parallel to the axis towards the load, along the equi-potentials, causing a parapotential flow [5]. This forms a Magnetically Insulted Transmission Line (MITL). Thus in MITL, electrons are diverted along equi-potentials insulating the anode and prevents from voltage breakdown. In MITL total current is given as in Eq. (10.8) [6].

$$I_0 = gI_\alpha\gamma_m\left(ln\left[\gamma_m + (\gamma_m^2 - 1)^{1/2}\right] + \frac{\gamma_0 - \gamma_m}{(\gamma_m^2 - 1)^{1/2}}\right) \tag{10.8}$$

Here

$g = {1}/{ln\left(\frac{r_0}{r_i}\right)}$, is geometric factor for co-axial transmission line

$I_\alpha = 8500\,A$, a constant and $\gamma = 1 + \frac{eV}{m_0c^2}$

At anode the $V = V_0$ and $\gamma = \gamma_0$. Thus

$$\gamma_0 = 1 + \frac{eV_0}{m_0c^2} \tag{10.9}$$

V_m is potential at any point in between cathode and anode and so γ_m. Plot of I_0 vs V_m shows, there is a minimum current, I_l at which $\gamma_m = \gamma_l$ as given in. Eq. (10.10). Relation between γ_l and γ_0 is given in Eq. (10.11).

$$I_l = gI_\alpha\gamma_l^3 ln\left[\gamma_l + (\gamma_l^2 - 1)^{1/2}\right] \tag{10.10}$$

$$\gamma_0 = \gamma_l + (\gamma_l^2 - 1)^{3/2} ln\left[\gamma_l + (\gamma_l^2 - 1)^{1/2}\right] \tag{10.11}$$

γ_l can be approximated in terms of γ_0 [7] as given in Eq. (10.12)

$$\gamma_l = \frac{12\gamma_0^{1/3}}{12+\ln\left(\frac{\gamma_0}{5.9314}\right)} \tag{10.12}$$

Eq. (10.12) is true for voltage adder up to 20 MV. From Eq. (10.12) we can find required γ_l for particular V_0. By knowing γ_l and keeping required load current to be I_l we can find geometric factor, g from (10.10). By knowing required outer radius, r_0 of the coaxial transmission line, we can find r_i i.e. inner shell radius.

10.4. Design of Inner Shell for LTD-1 MV

With the above method of designing inner shell, we have the inner shell diameters for LTD-1 MV as given in Table 10.2 for constant diameter in each module. This shows, for cavity#1, the required vacuum impedance is 1 Ω, but the calculated value is ~10.5 Ω. This implies ~28% of the cavity current is flowing through load as impedance due to magnetic core is ~4 Ω which is in parallel with load. This is very low efficient system. Thus, the design with the constant diameter of the inner shell in each module can't be adopted.

Table 10.2. Modified inner shell diameter.

Module No.	Module Voltage	Inner shell diameter	Co-axial Impedance
1	0.5 MV	226 mm	10.5 Ω
2	1.0 MV	202 mm	17.2 Ω
3	1.5 MV	181 mm	23.8 Ω
4	2.0 MV	163 mm	30.1 Ω
5	2.5 MV	148 mm	35.8 Ω
6	3.0 MV	134 mm	41.8 Ω

We need to go with conical inner shell with reducing radius. The diameter of the inner shell for few cavities is shown in Table 10.3. This shows, for conical inner shell, the impedance of the first cavity is 3.7 Ω in conical inner shell, instead of 10.5 Ω constant diameter inner shell in each module. So the adopted inner shell geometry is reducing conical geometry in each shell.

Table 10.3. Diameter of Conical Inner Shell.

Cavity No.	Inner Shell Diameter (mm)	Impedance (Ω)	E-field (kV/mm)
1	253	3.7	12.9
5	226	10.5	25.4
10	202	17.2	10.6
15	181	23.8	41.8
20	163	30.1	49.0
25	148	35.9	56.5
30	134	41.8	64.2

10.4.1. Design Simulation

Particle-in-cell simulation has been done of the designed 10 cavity LTD-1 MV. XOOPIC™ code has been used to see the magnetic insulation of the geometry. XOOPIC is X11 based GUI interface of OOPIC (Object Oriented Particle In Cell) code developed by University of California, Berkeley. This is a 2D PIC code with electrostatic and electromagnetic field solver having support for x-y and r-z geometries. The code simulates physical system that includes plasmas, beams of charged particles, externally generated electrical and magnetic fields, low-to-moderate density neutral gases with various boundary conditions [8].

10.4.2. Input File Preparation

An input file for XOOPIC code has been created by following way. LTD-1 MV is having 10 cavities. Figure 10.3 shows the overall diagram of the input file. Each cavity has been defined with two outer conductor rings of diameter 269 mm and length of 70 mm. Each ring is separated by dielectric ring of 20 mm thick and 45° angular surface. The dielectric is having dielectric constant of 2.3. So each cavity length is 160 mm. Each cavity is separated from its previous one by cavity length. 5 nos. of such cavities are kept one after another comprising a module. Total cavity length in each module is 800 mm. The end conductor ring of fifth cavity in each module has been extended by 200 mm to make the module length of 1000 mm. The second module (comprising 6th to 10th cavities) outer ring is replica of those of first module but shifted by module length along the z direction.

The inner shell is a conductor ring having diameter as given in Table 10.3. The diameter is constant along each cavity length. Also at the module transition length of 200 mm the inner shell diameter is fixed at initial shell diameter of next module. The inner shell is shorted with outer ring by a conductor annular disk at the initial end of the 1st cavity. The diode is designed to have an impedance of 10 Ω, so that total 100 kA current flows in the diode. Also the diode cathode diameter is kept as a continuation of the inner shell which corresponds to 11th cavity. Thus the diode gap is calculated to be 30 mm for 10 Ω impedance using Child-Langmuir law for planar diode [9].

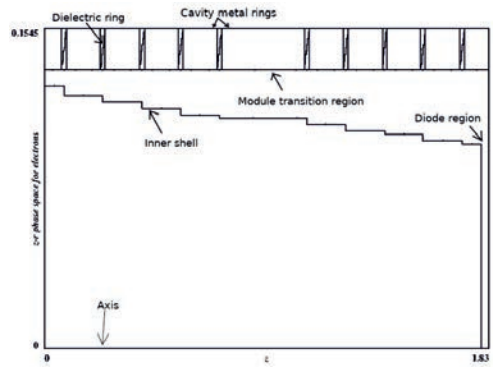
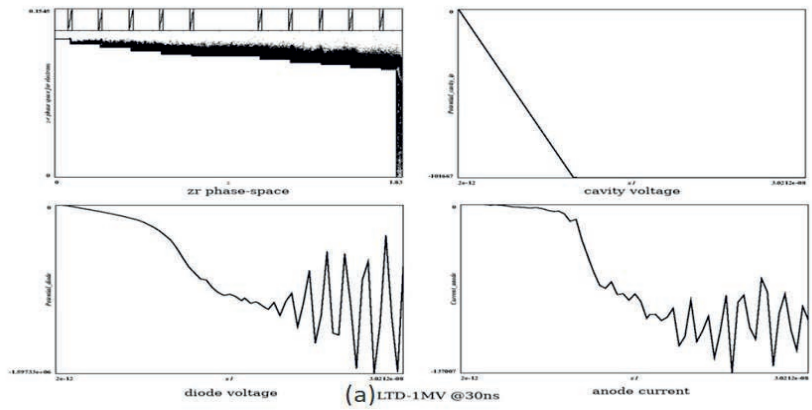


Figure 10.3. Overall diagram of LTD-1 MV as per input file.

Each cavity is given a pulse of peak voltage 100 kV, rise time 10 ns, pulse width 60 ns and fall time 10 ns. So, for 10 cavities, the output voltage should have 1 MV, which is the specified output of LTD-1 MV. All the cavities have been excited simultaneously without any defined delay among them. Also the inner shell has been defined as Field emitter only. This is space charge limited field emitter having zero threshold electric field [10]. The region has been considered to be in complete vacuum, that is, no other background particles are present in the region. Only electrons have been considered to be charged particles. No other ions have been considered to be present. The ratio of actual to computed particles have been chosen to be 10^{10}. The time resolution is chosen as 1 ps. Some diagnostic ports have been defined as (i) Cavity voltage is the voltage input across the cavity, (ii) Diode voltage is the total voltage across the diode gap and (iii) Anode current is the total current at the diode anode.

10.4.3. Results

Data has been saved for 30 ns and 80 ns and shown in Figure 10.4. The phase-space diagrams at various time intervals are shown in Figure 10.5. Figure 10.4(a) & 10.4(b) show the input cavity voltage at different time interval as per the specified input as given in previous section. Both the figures (a) & (b) show the average diode voltage ~1 MV and average diode current ~100 kA at 30 ns and 80 ns. Also it is found from the simulation results, after 70 ns (the total time of operation) the anode current and diode voltages are decreasing, which is at par our design. Because of zero threshold electric field chosen for cathode material, electrons start emitting from cathode at t = 0 ns. This is evident at phase-space diagram of 2 ns as shown in Figure 10.5(a). Parapotential flow of electrons is evident at 10 ns (Figure 10.5(b)) of application of voltage. All the electrons, starting from cathode surface moves towards the diode load instead of anode inner surface till 75 ns (Figure 10.5(c), 10.5(d)) from start. This is due to termination of input pulse at 70 ns. So, magnetic insulation is evident during the application of pulse.



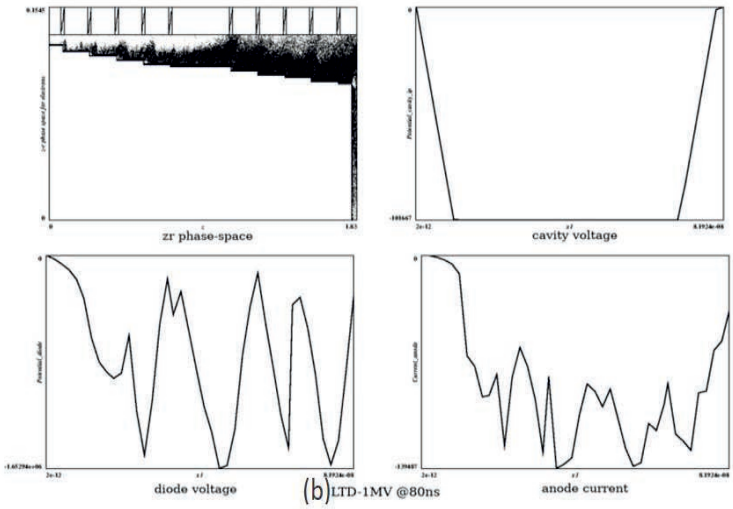


Figure 10.4. Simulated z-r phase space diagram of electrons, input cavity voltage, output diode voltage and anode current of LTD 1- MV at two time intervals (a) 30 ns, (b) 80 ns.

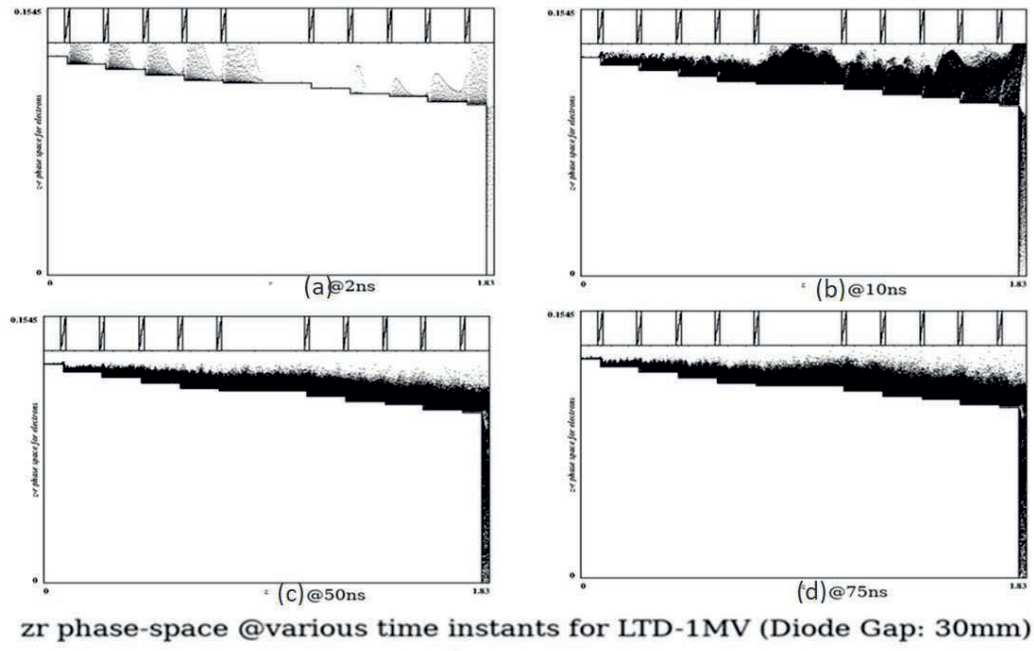


Figure 10.5. Phase-space diagram of electrons at various time intervals (a) 2 ns, (b) 10 ns, (c) 50 ns and (d) 75 ns.

10.5. Summary

Electrically, LTD scheme is an ingenious mix of conventional high voltage transformer coupling and 'Marx' staging techniques to generate voltage and current in the range of few MV's (Mega-Volts) and few hundreds of kilo-Amperes, respectively in typical loads of ~30 to 50 Ohms. LTD scheme can also be used in matched load conditions for the generation of Mega-Ampere currents for Z-Pinch and inertial fusion energy drivers. This chapter explains the methods for parameter selection of LTD-1 MV system and design of vacuum transmission line using Magnetically Insulated Transmission Line (MITL) topology.

References

[1] M. G. Mazarakis et al. "Linear Transformer Driver (LTD) Development at Sandia National Laboratory", IEEE Pulsed Power Conference: 138-145, 2005.

[2] D. Matia et al. "A 15 KA Linear Transformer Driver", IEEE International Pulsed Power Conference: 926-929, 2009.

[3] M. S. Rylko et al. "Magnetic Material Selection for High Power High Frequency Inductors in DC-DC Converters", 24th Annual IEEE Applied Power Electronics Conference and Exposition (APEC): 2043-2049, 2009.

[4] G.A. Mesyats, "Pulsed Power", Springer Publication, ISBN: 0-306-48653-9, 2004

[5] B. Bernstein and I Smith, "AURORA, AN ELECTRON ACCELERATOR", IEEE Trans. Nucl. Sci., 20(3), 294, 1973

[6] John M Creedon, "Relativistic Brillouin flow in the high ν/γ diode", Jnl of Appl Phys, 46(7), 1975

[7] M.G. Mazarakis et. al., "SMILE: A SELF MAGNETICALLY INSULATED TRANSMISSION LINE ADDER FOR THE 8-STAGE RADLAC II ACCELERATOR", IEEE PPC, 1991

[8] "OOPIC ProTM Object-Oriented Partcicle-in-Cell Simulation, User's Manual", Tech-X Corporation, 2004

[9] R.B. Miller, "An Introduction to Physics of Intense Charged Particle Beams", Springer Publication, ISBN: 978-1-4684-1130-0, 1982

[10] OOPIC Pro™ User's Manual, Version 1.0, Tech-X Corporation, http://www.txcorp.com, Copyright 1998-2004 Tech-X Corporation August 11, 2004